Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	4880	(plurality with (chip or die)) and mold and (cavity or void or space) and (pressure or resilient or elastic)	US-PGPUB; USPAT	OR	ON	2005/03/12 09:30
L2	2342	1 and (simultaneously)	US-PGPUB; USPAT	OR	ON	2005/03/12 09:23
L3	654	2 and (individually)	US-PGPUB; USPAT	OR	ON	2005/03/12 09:24
L4	525	3 and @ad<"20020927"	US-PGPUB; USPAT	OR	ON	2005/03/12 09:26
L5	1330	264/272.17,511,272.15,276.ccls. and @ad<"20020927"	US-PGPUB; USPAT	OR	ON	2005/03/12 09:26
L6	479	5 and (simultaneously)	US-PGPUB; USPAT	OR	ON	2005/03/12 09:26
L7	73	6 and (individually)	US-PGPUB; USPAT	OR	ON	2005/03/12 09:26
L8	832	264/102.ccls. and @ad<"20020927"	US-PGPUB; USPAT	OR	ON	2005/03/12 09:27
L9	284	8 and (simultaneously)	US-PGPUB; USPAT	OR	ON	2005/03/12 09:30
L10	39	9 and (individually)	US-PGPUB; USPAT	OR	ON	2005/03/12 09:31
L11	39	10 and @ad<"20020927"	US-PGPUB; USPAT	OR	ON	2005/03/12 09:27
L12	35	11 not 7	US-PGPUB; USPAT	OR	ON	2005/03/12 09:27
L13	3319	438/106-108,127.ccls. and @ad<"20020927"	US-PGPUB; USPAT	OR	ON	2005/03/12 09:28
L14	1078	13 and (simultaneously)	US-PGPUB; USPAT	OR	ON	2005/03/12 09:28
L15	241	14 and (individually)	US-PGPUB; USPAT	OR	ON	2005/03/12 09:28
L16	1251	(plurality with (chip or die)) and mold and (cavity or void or space) and (pressure or resilient or elastic)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/12 09:30
L17	523	16 and (simultaneously)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/12 09:30
L18	84	17 and (individually)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/12 09:31

US-PAT-NO: 6750083

DOCUMENT-IDENTIFIER: US 6750083 B2

TITLE: Method of masking microelectronic semiconductor chips with protective caps

---------- KWIC ---------

Brief Summary Text - BSTX (4):

Semiconductor chips are normally packaged in a protective layer or layers to protect the chip and its wire bonds from atmospheric and mechanical damage. Existing packaging systems typically use epoxy molding and thermal curing to create a solid protective layer around the chip. This is normally carried out on **individually** diced chips bonded to lead frames and so must be done many times for each wafer. Alternative methods of packaging include hermetically sealed metal or ceramic packages, and array packages such as ball grid array (BGA) and pin grid array (PGA) packages. Recently wafer scale packaging (WSP) has started to be used. This is carried out at the wafer stage before the chips are separated. The use of molding and curing techniques subjects the wafer to both mechanical and thermal stresses. In addition the protective cap so formed is a solid piece of material and so cannot be used for MEMS devices, since the MEMS device would be rendered inoperable by the polymer material. Existing packaging systems for MEMS devices include thematically sealed packages for individual devices, or use silicon or glass wafer scale packaging, both of which are relatively high cost operation.

Drawing Description Text - DRTX (13):

FIG. 13 shows the device of FIG. 10 after molding has finished and just before one side of the **mold** is released from the other side.

Drawing Description Text - DRTX (16):

FIG. 15 shows a cross sectional side view of the device after one of the **molds** has been partially removed.

Drawing Description Text - DRTX (17):

FIG. 16 shows a cross sectional side view of the device after one of the **molds** has been fully removed.

Drawing Description Text - DRTX (20):

FIG. 19 shows a cross sectional side view of the device at the commencement of application to a wafer and removal of the second **mold**.

Detailed Description Text - DETX (2):

Referring to FIGS. 1 and 2 there is show a prior art method of forming protective caps on semiconductor wafers on a wafer scale. A semiconductor wafer 10 is clamped against a **mold** 12 having **cavities** 14 formed therein and a liquid polymer material 16 is injected into the **cavities** 14. The polymer material sets to form solid protective caps 18. The wafer is then singulated using a wafer saw. This technique is not applicable to wafers having MEMS devices formed thereon as the liquid polymer material will surround the MEMS devices and stop them from working.

Detailed Description Text - DETX (3):

FIG. 3 shows the present prior art technique for protecting MEMS devices. The MEMS chip 20 including the MEMS devices 24, shown symbolically, is bonded to a silicon wafer 26. This may be carried out at the individual chip stage or at the wafer stage. The wafer 26 is typically etched using a crystallographic anisotropic etch using an etchant such as KOH to form a series of recesses 28 which correspond to the locations of the MEMS devices. The wafers 26 are carefully aligned with the MEMS wafer 20 and bonded thereto. While this can be an effective means of packaging MEMS devices, it is expensive as it requires an extra silicon (or sometimes glass) wafer, which must be etched to form the **cavities**.

Detailed Description Text - DETX (4):

FIG. 4 shows a MEMS wafer 30 having surface MEMS 32 formed thereon. A hollow protective cap 34 of thermoplastic material made and bonded to the wafer 30 according to the invention is provided so as to form a mechanical and atmospheric protective barrier for the MEMS devices. The cap 34 forms a **cavity** 36 with the wafer to allow the MEMS device(s) to operate.

Detailed Description Text - DETX (7):

An array of caps 48 is formed using conventional injection molding methods and steel **mold** tools 50 & 52. The caps are supported on a sprule 54 at the same nominal spacing as the groups 42. Using this method will almost invariably lead to misalignment with resulting destruction of MEMS devices, as shown in FIG. 7. In FIG. 7 the cap 48a has been aligned correctly with its group of MEMS devices 42a. However the spacing between the caps is greater than the spacing of the groups so that cap 48b is not aligned correctly, but does not destroy any of the MEMS devices of its respective group 42b. However, the caps 44c & d are sufficiently misaligned that the perimeter walls of the

caps overlay one or more of the MEMS devices 44, destroying their functionality.

Detailed Description Text - DETX (14):

It is not essential that the **mold** wafers only contact on surfaces which have not been etched. Nor is it essential that the central portion is defined by a recess in only one **mold** or that the perimeter walls be defined by a groove or recess in only one **mold**. The effective split line between the **molds** may be located at any position desired and need not be planar. However, planarity of the split line will typically simplify fabrication of the **molds**.

Detailed Description Text - DETX (15):

The assembly 100 also includes an upper release or eject wafer 118 and a lower release or eject wafer 120. These upper and lower release wafers are silicon wafers which have been processed utilizing conventional lithography and deep silicon etching techniques to have a series of release pins 122 and 124 respectively. The upper and lower **mold** wafers 102 & 104 are formed with corresponding holes 126 & 128 respectively which receive the pins 122 & 124. The upper holes 126 are located generally toward the center or axis of each recess 106 whilst the lower holes 128 are located in the grooves 112. However the location of the holes 126 and 128 is not especially critical and they may be placed as required for ejection of the molded caps.

Detailed Description Text - DETX (16):

The release pins 122 & 124 have a length greater than the depth of the corresponding holes. When the free ends of the pins 122 align with the inner ends of the holes 126, there is a gap 130 between the upper **mold** wafer 102 and the upper release wafer 118. In this embodiment the length of the lower pins 124 is the same as the thickness of the lower **mold** wafer 104. However the length of the pins 124 may be greater than the thickness of the wafer or it may be less. When the length of the pins 124 is less than the maximum thickness of the lower wafer 104 it needs to be greater than the depth of the holes 128, i.e. at least the reduced thickness of the wafer 104 at the grooves 112. The lower wafers 104 and 120 are positioned with the pins 124 part way inserted in the holes 128 but not extending beyond the holes 128 into the grooves 112 and with a gap 132 between the two wafers. The pins 124 preferably extend to be flush with the ends of the holes so as to form a substantially planar base to the groove 112.

Detailed Description Text - DETX (17):

The thickness of the **mold** and release wafers is about 800 microns whilst the gaps 130 and 132 are of the order of 10 to 100 microns in thickness. However

this is not critical.

Detailed Description Text - DETX (18):

The **mold** tools are preferably etched using cryogenic deep silicon etching rather than Bosch etching as to produce a smoother etch. Bosch etching produces scalloping of etched side walls, such as the side walls of the pin and cap recesses. The scalloping makes the release of the **molds** from the molded material more difficult. In comparison, using a cryogenic etch results in much smother etched walls, with easier **mold** release.

Detailed Description Text - DETX (20):

The assembly is mechanically pressed together in the machine but it will be appreciated that the **mold** wafers may be urged toward each other to deform the thermoplastic sheet by applying an above ambient **pressure** to the gaps 130 & 132. Alternatively other means may be used.

Detailed Description Text - DETX (21):

The sheet 134 may be heated by conduction but is preferably heated by radiation and preferably by using infrared radiation, as indicated by arrows 136 in FIG. 12. A combination of conductive and radiant heating may be used. The **mold** and release wafers 102 &104 and 118 & 120 respectively are formed of silicon, which is substantially transparent to infrared light of a wavelength in the range of about 1000 nm to about 5000 nm. The material 134 chosen either intrinsically absorbs light within this wavelength range or is doped so as to absorb light within this wavelength range. If the material 134 does not intrinsically absorb within this range, a suitable dopant is "carbon black" (amorphous carbon particles) which absorbs light at these wavelengths. Other suitable dopants may be used.

Detailed Description Text - DETX (22):

The sheet 134 is placed between the two **mold** wafers and exposed to infrared light at a suitable wavelength, as indicated by arrows 136. The infrared radiation is preferably supplied from both sides of the wafers and the sheet 134 to provide symmetrical heating, but this is not essential and the infrared radiation may be supplied from only one side. Because the silicon wafers are transparent to the infrared radiation, the infrared radiation passes through the wafers and is absorbed by the sheet 134. After heating to a suitable temperature the **mold** wafers may then be urged together to deform the sheet 134. The wafers may be pressed together whilst the sheet 134 is being heated rather than waiting for the sheet 134 to be fully heated, particularly if conductive heating is being used. If a material other then silicon is used heating of the sheet 134 may be achieved using electromagnetic radiation at other wavelengths

to which the material used is substantially transparent.

Detailed Description Text - DETX (23):
When processed in a wafer bonding machine the sheet 134 is molded to the shape of the **cavity** defined by the recess 106 and the groove 112. The material is also substantially squeezed out of the gap between the two portions 114 & 116, as indicated by arrows 142 in FIG. 13a, to form a series of caps 138

Detailed Description Text - DETX (25):
It is not essential that the **mold** wafers or the release wafers be made of semiconductor materials or that they be processed using conventional lithography and deep silicon etching methods. Other materials and methods may be used if desired. However, the use of similar materials to the semiconductor wafers provides better accuracy since temperature changes have less effect. Also lithography and deep silicon etching methods are well understood and provide the degree of accuracy required. In addition, the one fabrication plant may be used for production of both the semiconductor devices and the molding apparatus.

Detailed Description Text - DETX (26):
It will be appreciated that the two **mold** wafers 102 & 104 will need to be shaped so that there is **space** for the material to move into as it is squeezed out from between the two wafers.

Detailed Description Text - DETX (27):
After forming of the protective caps 138 it is preferred to remove the lower **mold** and release wafers 104 & 120 whilst leaving the material 134 still attached to the upper **mold** wafer 102. A vacuum is applied to the gap 132 between the lower **mold** and release wafers. The release wafers 118 & 120 are mounted in the assembly so as to be immovable whilst the **mold** wafers 102 & 104 are movable perpendicular to the general plane of the wafers. Accordingly, the lower **mold** wafer 104 is drawn downwards to the release wafer 120. The pins 124 of the release wafer 120 firmly press against the material 134 and so retain the material 134 in position and prevent it moving downwards with the lower **mold** wafer 124. The configuration of the assembly 100 after this stage is shown in FIG. 15.

Detailed Description Text - DETX (28):
The lower release wafer 120 now only contacts the material 134 by pins 124 and so it is now relatively easy to remove the lower release wafer 120 from contact with the material 134 without dislodging the material from the upper **mold** wafer 102. This is done and the assembly is then in the configuration

shown in FIG. 16, with the material 134 exposed for further processing and attachment to a wafer.

Detailed Description Text - DETX (29):

Whilst still attached to the upper **mold,** the sheet 134 is then subject to an etch, preferably an oxygen plasma etch, from below, to remove the thin layer 140 of material, as shown in FIG. 17. The etch has little effect on the rest of the material due to the significant greater in thickness of the rest of the material. The etched assembly is shown in FIG. 18.

Detailed Description Text - DETX (30):

The assembly is then placed over a wafer 144 having a number of chips formed on the wafer. Each **chip has a plurality** of MEMS devices 146. The components are aligned and then placed in a conventional wafer bonding machine, such as an EV 501 to bond the caps 138 to the wafer. The array of chips is positioned so that each cap overlays part or all of a chip. The devices are shown symbolically and may be MEMS devices, MOEMS devices, other micro fabricated devices, passive electronic elements or conventional semiconductor devices.

Detailed Description Text - DETX (31):

The assembly is removed from the wafer bonding machine and a vacuum is then applied to the upper gap 130 so as to draw the upper **mold** wafer 102 up toward the upper release wafer 118. Similar to the release of the lower **mold** wafer, the caps 138 are held in place by the pins 122 of the upper release wafer. Thus the chance of accidental detachment of any of the caps from the wafer due to the act of removing the upper **mold** wafer is reduced, if not totally prevented.

Detailed Description Text - DETX (34):

FIG. 22 shows a technique for providing protective caps for both the upper and lower surfaces. The figure shows a wafer 150 upon which have been formed a series of MEMS device chips 153 on an upper surface 154. Each chip 153 includes one or more MEMS devices 152 and optionally other micro fabricated elements. A first set of protective caps 156 have been formed on the upper surface 154 as per the techniques of the invention previously described. The bond pads 158 of the individual chips 153 are on the upper surface 154 and are not covered by the protective caps 156. A second set of protective caps 160 have been formed on the lower surface 162 of the wafer as per the techniques of the invention previously described. The first and second sets of protective caps may be applied to the wafer sequentially or may be applied to the wafer **simultaneously**. The order of application is not important. The second set of caps 160 are located under each chip 153 but are larger than the first set 156

and extend under and beyond the bond pads 158.

Detailed Description Text - DETX (36):

It will be appreciated that the provision of the second set of caps is only a necessity where a hollow **space** is required; if a second set of caps is unnecessary or undesirable, a resist may be coated onto the lower surface with a grid pattern to leave areas between the chips exposed for deep etching.